

JSS Mahavidyapeetha JSS Academy of Technical Education, Noida





FACULTY PROFILE

1. Personal Details

NAME	Dr. Ritesh Kumar Jaiswal	
DEPARTMENT	ELECTRONICS AND COMMUNICATION ENGINEERING	
DESIGNATION	ASSISTANT PROFESSOR	
PHONE	7071244802	
EMAIL ID	riteshjaiswal@jssaten.ac.in	
Date of Joining (JSSATEN)	06/05/2022	

2. Experience

Total Experience in Years:-6 Y 6 Months Teaching:- 6 Y Months	Industry:- 0	Research:-0
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3. Qualifications

COURSES	SPECIALIZATION	Year of Award	INSTITUTION	UNIVERSITY
B.E.	Electronics and Telecommunication Engineering (E&TC)	2007	RKGIT Ghaziabad	U.P.T.U. Lucknow
M.Tech.	Digital Systems (ECE)	9 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7		G. B. T. U. Lucknow
Ph.D.	VLSI (ECE)	Motilal Nehro National Institute		Motilal Nehru National Institute of Technology Allahabad, Prayagraj
Post Doc.	-	-	-	-

4. Research & Publications

Papers Published in Web of Science indexed	International: 03	National: 00		
Journals				
Papers Published in				
SCOPUS indexed	International: 00	National: 00		
Journals				
Papers Published in	International: 00	National: 00		
other Journals	international. 00	National, 00		
Papers Presented in				
Conferences /	International: 07	National: 00		
Symposium				
Books / Book chapters				
Published		-		

5. Research Guidance

PhD Guide? Give field No & University		University: NIL
PhDs / Projects Guided	Ph.D. Awarded: Guiding: NIL	Projects at Master's Level: -00 Projects at Bachelor's Level: 5

6. Grants

i. Funds Received (Projects)

Project Name	Grant Amount	Date of receiving the Grant	Duration in Years	Grant issuing authority/ Body / Organization
-	-	-	Ī	-

ii. Patents

Sl. No.	Title Details	Details of award of patent / Filed
-	-	_

iii. Consultancy

Title of the work	Amount in Rs.	Date of receiving the Grant	Duration	Grant issuing authority/ Body / Organization
-	1	-	-	-

7. Awards Received

Awards	
"Best Paper Award"	-

8. Publications

i. International Journals

Sl. No	Title of the paper	Name(s) of Author(s)		Volume No. Issue No. Year	WOS / Scopus / Both	Impact Factor	Publisher
1	Perspective and Opportunities of Modulo 2^n- 1 Multipliers in Residue Number System: A Review	Raj Kumar, Ritesh Kumar Jaiswal, and Ram Awadh Mishra.	Journal of Circuits, Systems and Computers	Vol. 29 no. 11, (2020), Page 2030008	Both	1.333	World Scientific
2	"Electronic Structure and Optical Properties of Gallium-Doped Hybrid Organic— Inorganic Lead Perovskites from First-Principles Calculations and Spectroscopic Limited Maximum Efficiencies"	Ritesh Kumar Jaiswal, Raj Kumar and Ram Awadh Mishra.	Journal of Circuits, Systems and Computers	Vol. 27 no. 5, (2018): Page 1850075	Both	1.333	World Scientific
3.	Area Efficient Sparse Modulo 2^n-3 Adder	Ritesh Kumar Jaiswal, Chatala Naveen Kumar and Ram Awadh Mishra.	Circuits and Systems	Vol. 7 no. 12 (2016): Page 4024			Scientific Research

ii. National Journals

Sl. No.	Title of the paper	Name(s) of Author(s)	Name of the Journal	Volume No. Issue No. Year	WOS / Scopus / Both	Impact Factor	Publisher
-	-	-	-	_	-	-	-

iii. Conferences

Sl. No.	Title of the paper	Name(s) of Author(s)	Name of the Conference	Volume No. Issue No. Year	WOS / Scopus	Impact Factor	Publisher
1	Design and	Manikanta, G.,	Advances in	Vol 1. 2,	Scopus		Springer

	Analysis of Self	R. A. Mishra,	VLSI,	pp. 627-		
	biased OTA for	N. A.	Communication,	637,		
	Low-Power Applications	Srivastava, and R. K. Jaiswal.	and Signal Processing	2020		
	Applications	IX. IX. Jaiswai.	Trocessing			
2	Efficient Design for High Speed and Low Area Reverse Converter for Moduli Set {2^{n}, 2^{2n}-1, 2^{2n}+1}	Kumar, Raj, Ritesh Kumar Jaiswal, and Ram Awadh Mishra.	International Conference on Electrical, Electronics and Computer Engineering (UPCON), AMU Aligarh International	Vol. 1. Pp. 1-6. 2019	Scopus	IEEE
3	Outage Probability of Device-to- Device Communication Underlaying Cellular Network over Nakagami/Rayleigh Fading Channels	Singh, Indrasen, R. K. Jaiswal, Varun Kumar, Rajiv Verma, N. P. Singh, and Ghanshyam Singh	Conference on Emerging Trends in Engineering and Technology- Signal and Information Processing (ICETET-SIP- 19) GHRCE Nagpur,	Vol. 1. Pp. 1-5. 2019	Scopus	IEEE
4	Linearity Enhancement of CMOS OTA for High Performance Applications	Prasad, Narendra, Nilesh Anand Srivastava, Ritesh Kumar Jaiswal, and Ram Awadh Mishra	5 th IEEE Uttar Pradesh Section International Conference on Electrical,	Vol. 1. Pp. 1-6. 2018	Scopus	IEEE
5.	Performance evaluation of digital and RNS based filter for fast DSP processors.	Jaiswal, R. K., Megha Bagre, and R. A. Mishra	International Conference on Emerging Trends in Computing and Communication Technologies (ICETCCT), GEHU Dehradun	Vol. 1. Pp. 1-4. 2017	Scopus	IEEE

6	New Area Efficient Modulo 2^n+1 Multiplier	Singh Premlata, Ritesh Jaiswa and R. A Mishra	SKM University	Vol. 1. Pp. 1-5. 2016		IEEE
7.	Performance analysis of SiGerC HBT	Jaiswal, Ritesh Kumar, and R. K Chauhan	Technology	Vol. 1. Pp. 1-5. 2010	Scopus	IEEE

iv. Workshops/Conferences Attended

Sl. No.	Name of the workshop / Conference	Organizer	Date	
1	FDP on Advanced Embedded System & Microelectronics (AESM-2016)	MNNIT Allahabad	14-20 July, 2016	
2	Workshop on Soft Skills (SS-2018)	MNNIT Allahabad	21-25 May 2018	
3	Short Term Course on Sub-micrometer Semiconductor Device to Circuit CoDesign and Modeling Techniques	Dr. B. R. Ambedkar National Institute of Technology Jalandhar	20-25 August 2020	
4	workshop on <i>Embedded System- An Application Driven Approach</i>	AICTE and ST Microelectronics and ARM	25-27 August 2021	
5	ATAL faculty development program on Recent Trends and Advances in Photonic Integrated Circuits and Its Applications	University Institute of Technology Himanchal Pradesh University	4 – 8 October 2021	
6	AICTE Recognized Faculty Development Programme on Arduino based system design using Tinker CAD Free Simulator	NITTR CHANDIGARH	20-24 June 2022	
7	Two weeks Faculty Development Program on "Emerging Technologies	Jamia Hamdard, New Delhi	1-14 August 2022	
8	Microsoft India & SAP India led Faculty Development Program on "Artificial Intelligence	TechSaksham Program	21-23 Dec 2022	

v. Workshops / Conference (Organized)

l. No.	me of the workshop / Conference	Organized by	Date	Role
1	Standardization & Intellectual property Rights (IPR), 7th GISFI	ITU and GISFI	2011	Volunteer
	meeting			

vi. Conference Attended (those sponsored by AICTE / ISTE/IETE/TEQIP or any other sponsoring body)

Sl. No.	Name of the workshop / Conference	Organizer	Date
1			
2			

9. Details of NPTEL / COURSERA courses completed

Sl. No.	Name of the subject	Organized by	Date of completion / Award	Grade / Marks
1	Microelectronics: Device to Circuits	NPTEL	Jul-Oct 2021	69%
2	LaTeX for Students, Engineers, and Scientists	IITBombayX	4 th December 2019	A+

10. M	0. Membership of Professional Bodies:					
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11. Any other information you will like to share about your professional experience

Qualified GATE in EC: 2006, 2014, 2020

Qualified UGC NET in Electronic Science: December 2015